

100 ↗

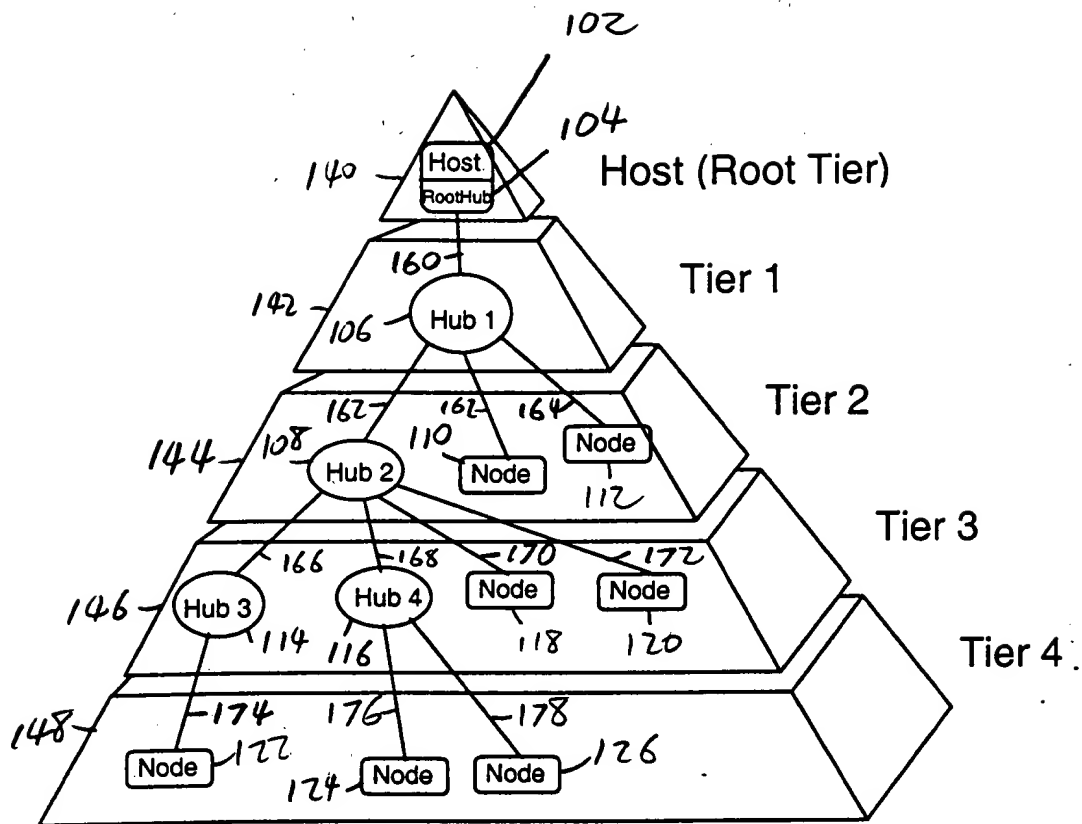


FIGURE 1

09540676-033100

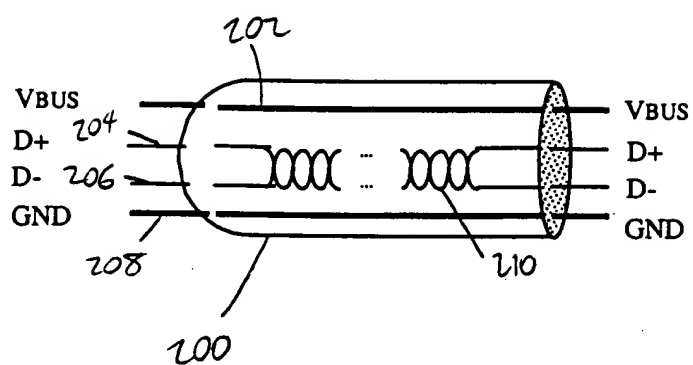
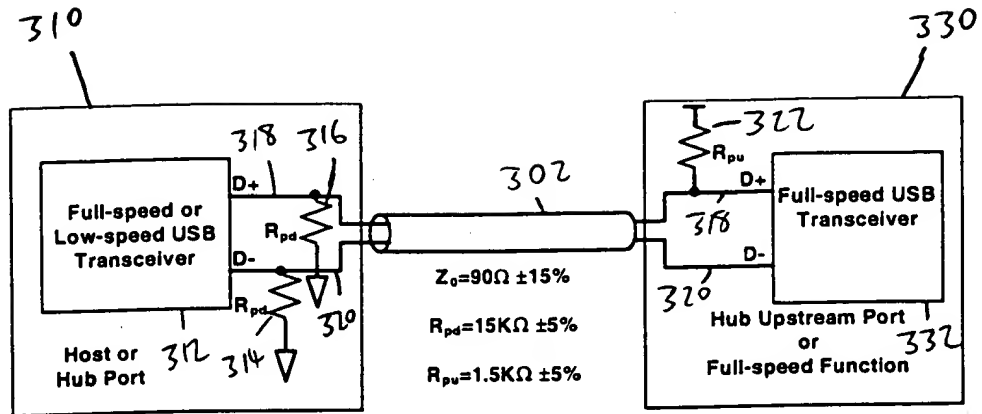
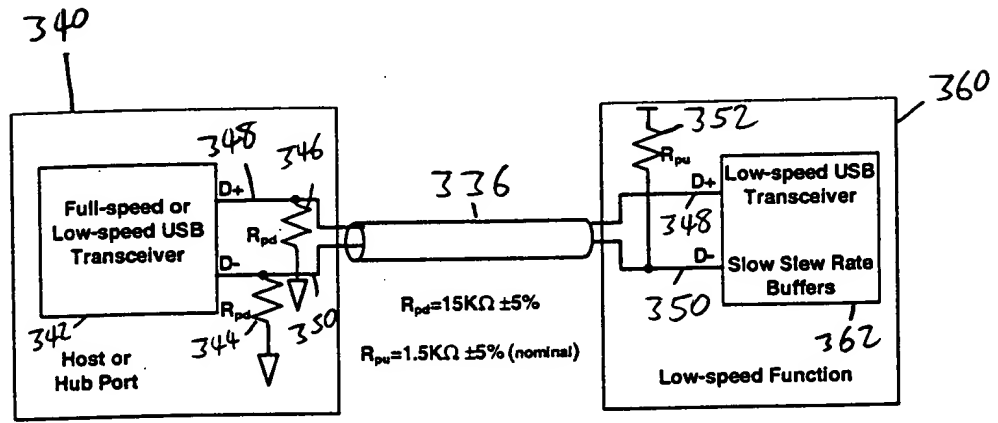


FIGURE 2



Full-speed Device Cable and Resistor Connections

FIGURE 3A



Low-speed Device Cable and Resistor Connections

FIGURE 3B

```
graph TD
    S0((State 0  
off)) -- "power on" --> S3((State 3  
normal  
standby))
    S3 -- "WAK# assert" --> S4((State 4  
attention  
required))
    S4 -- "WAK# deassert" --> S3
    S3 -- "logical attach" --> S1((State 1  
normal  
operating))
    S1 -- "logical detach" --> S3
```

\_\_\_\_\_

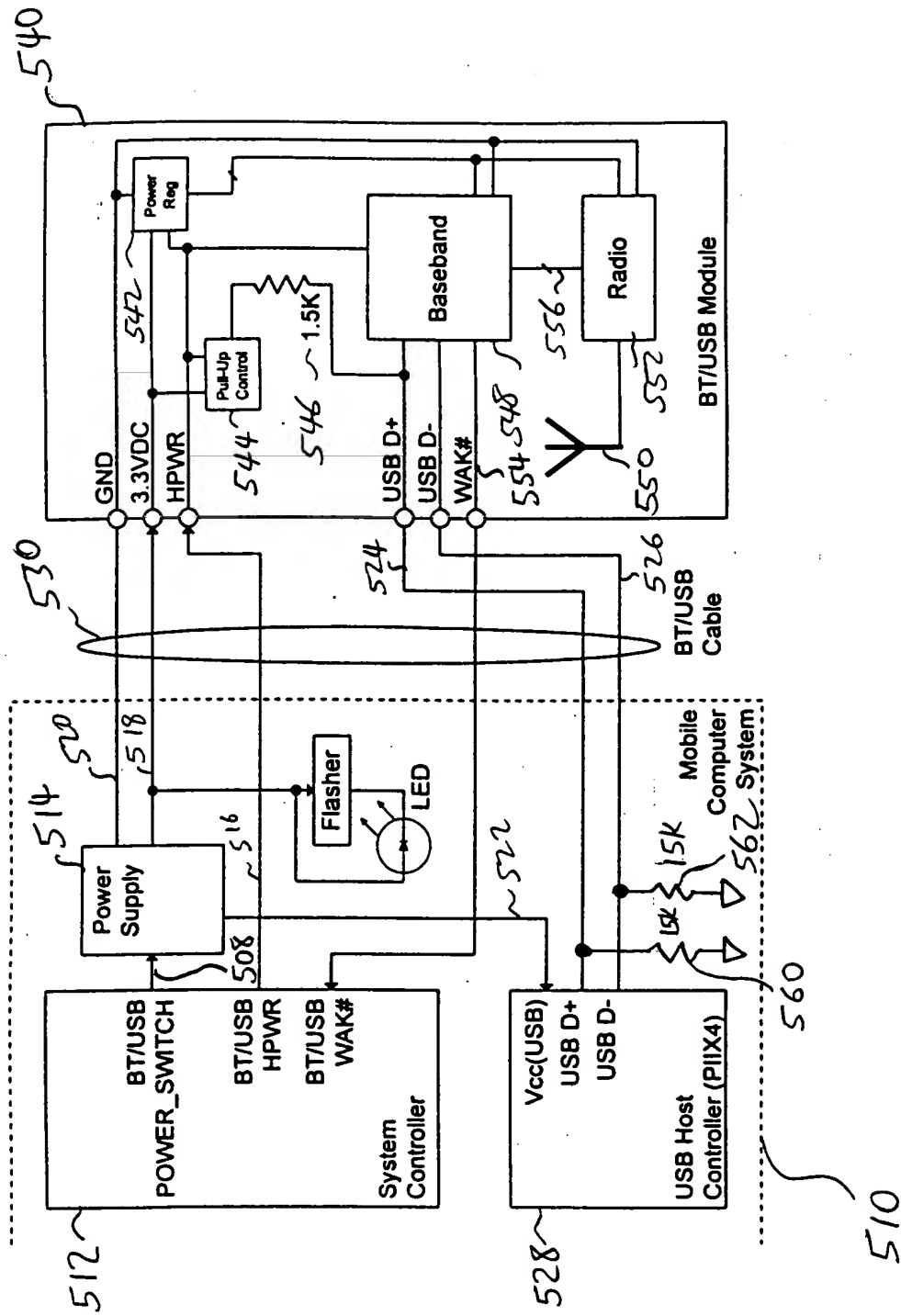


FIGURE 5

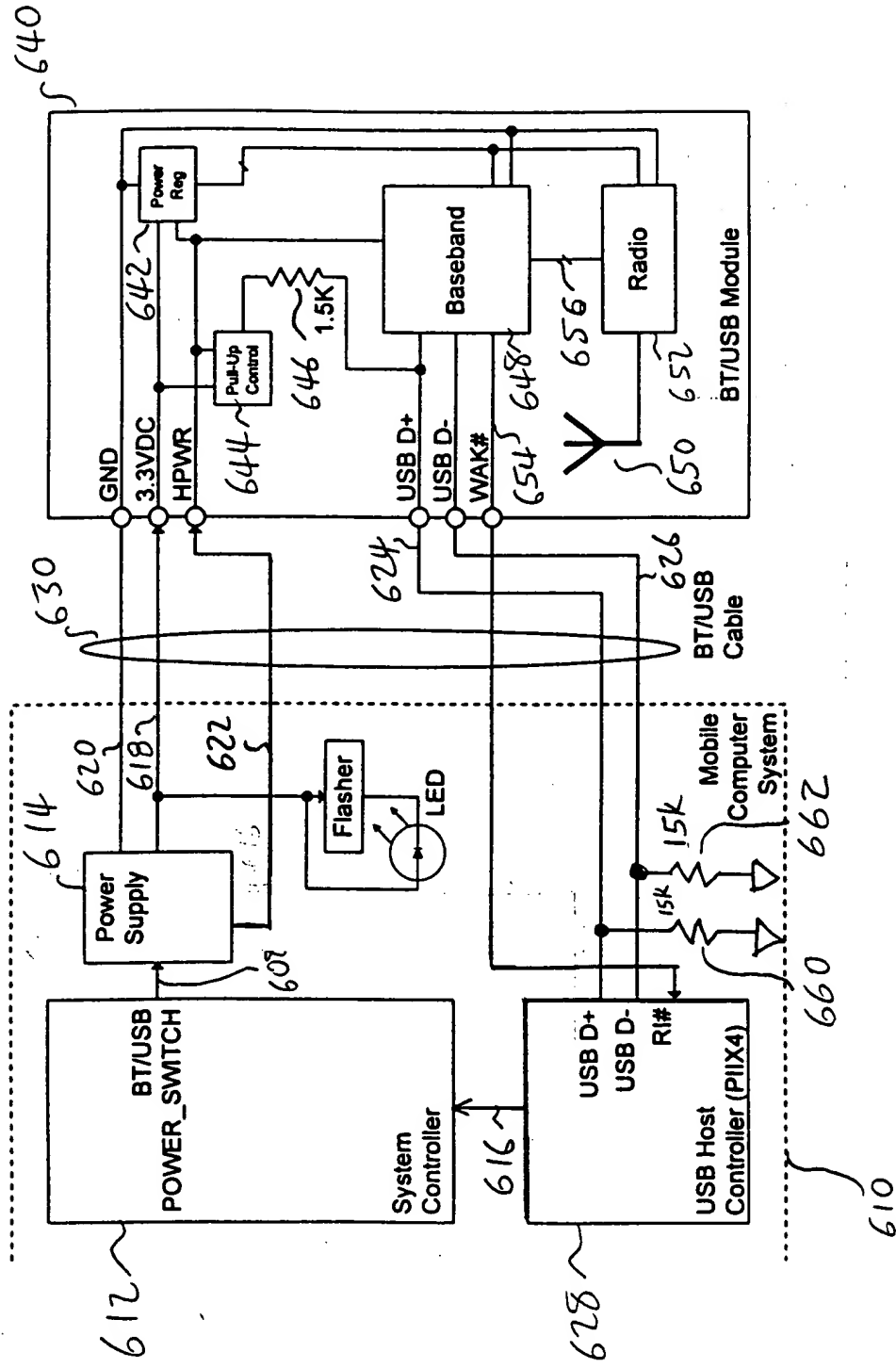


FIGURE 6

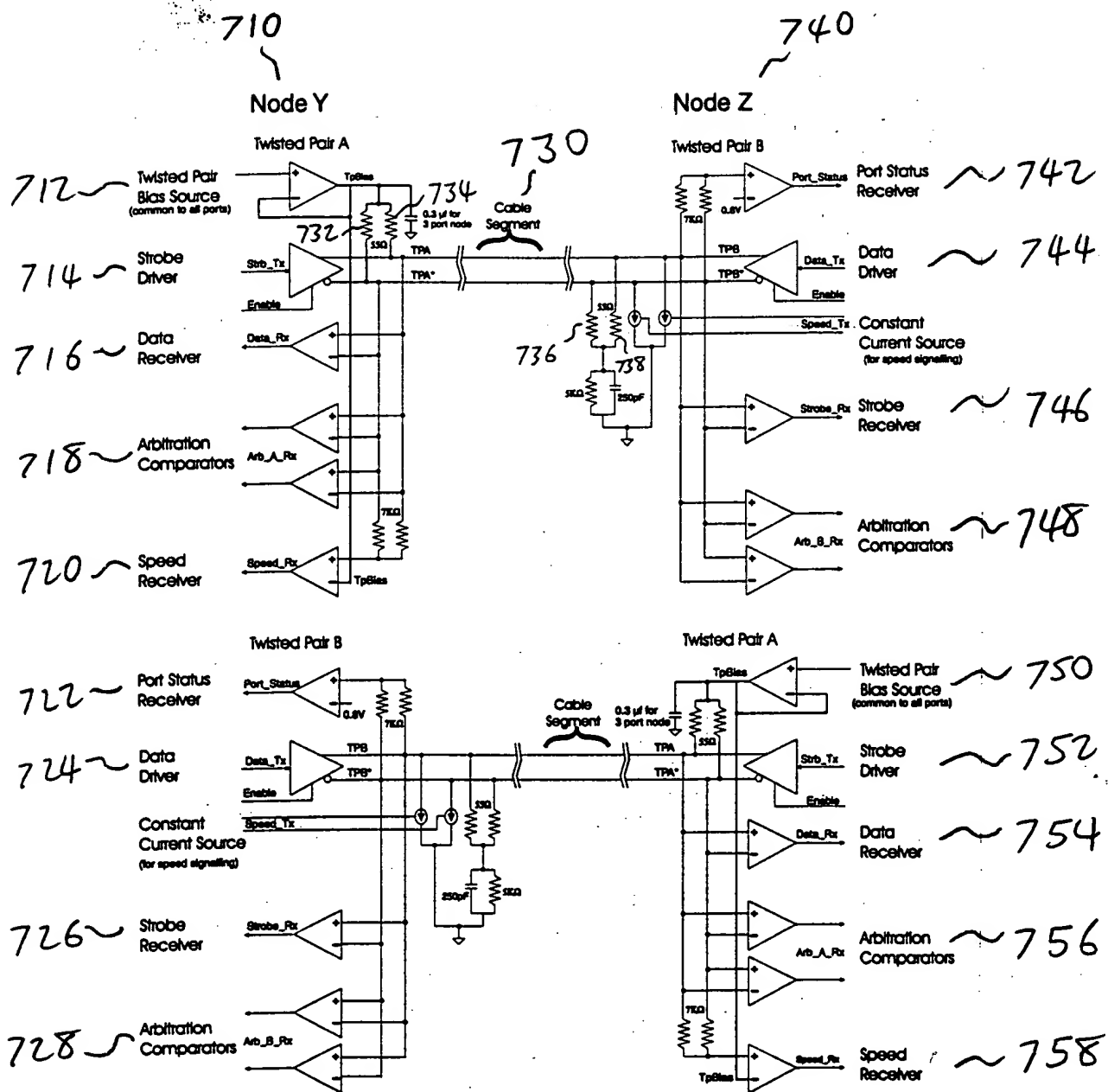
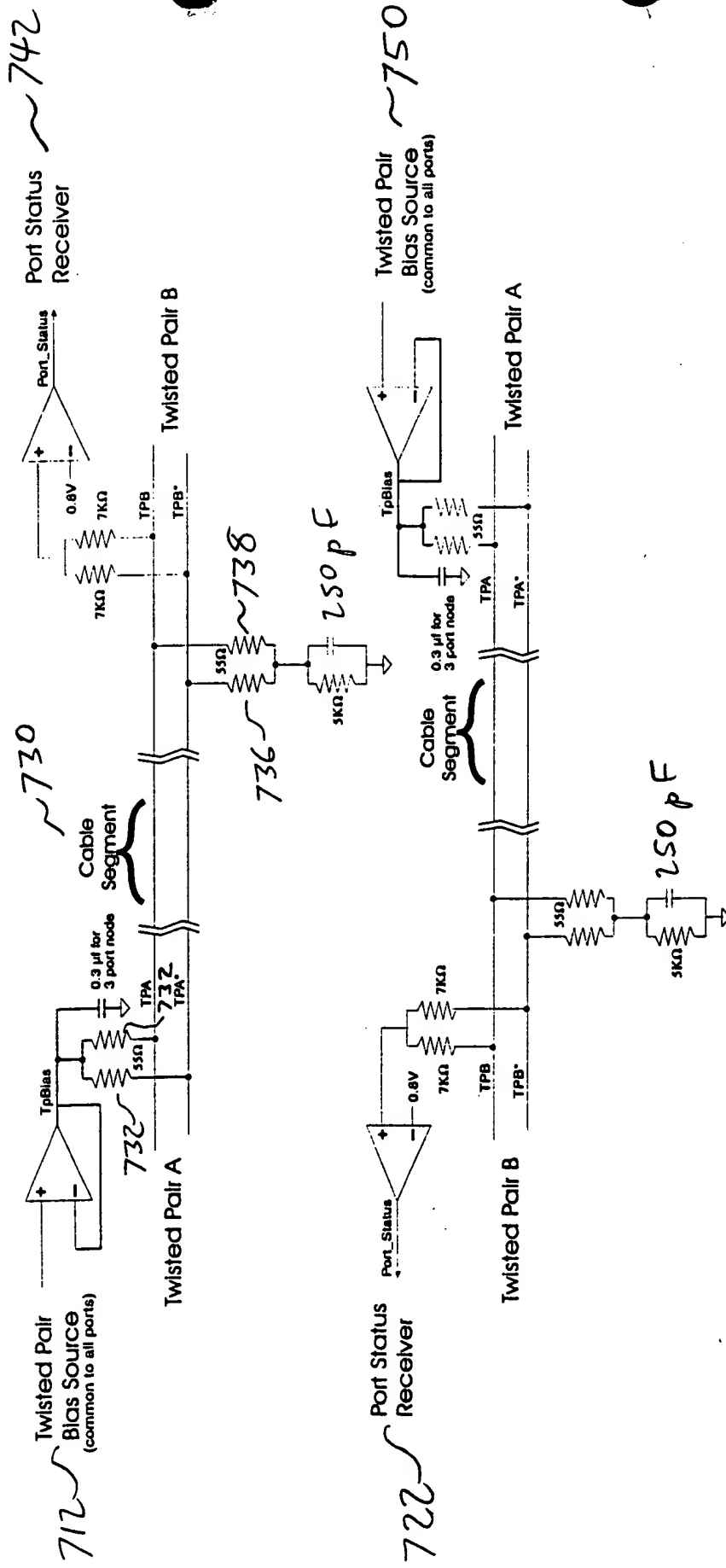
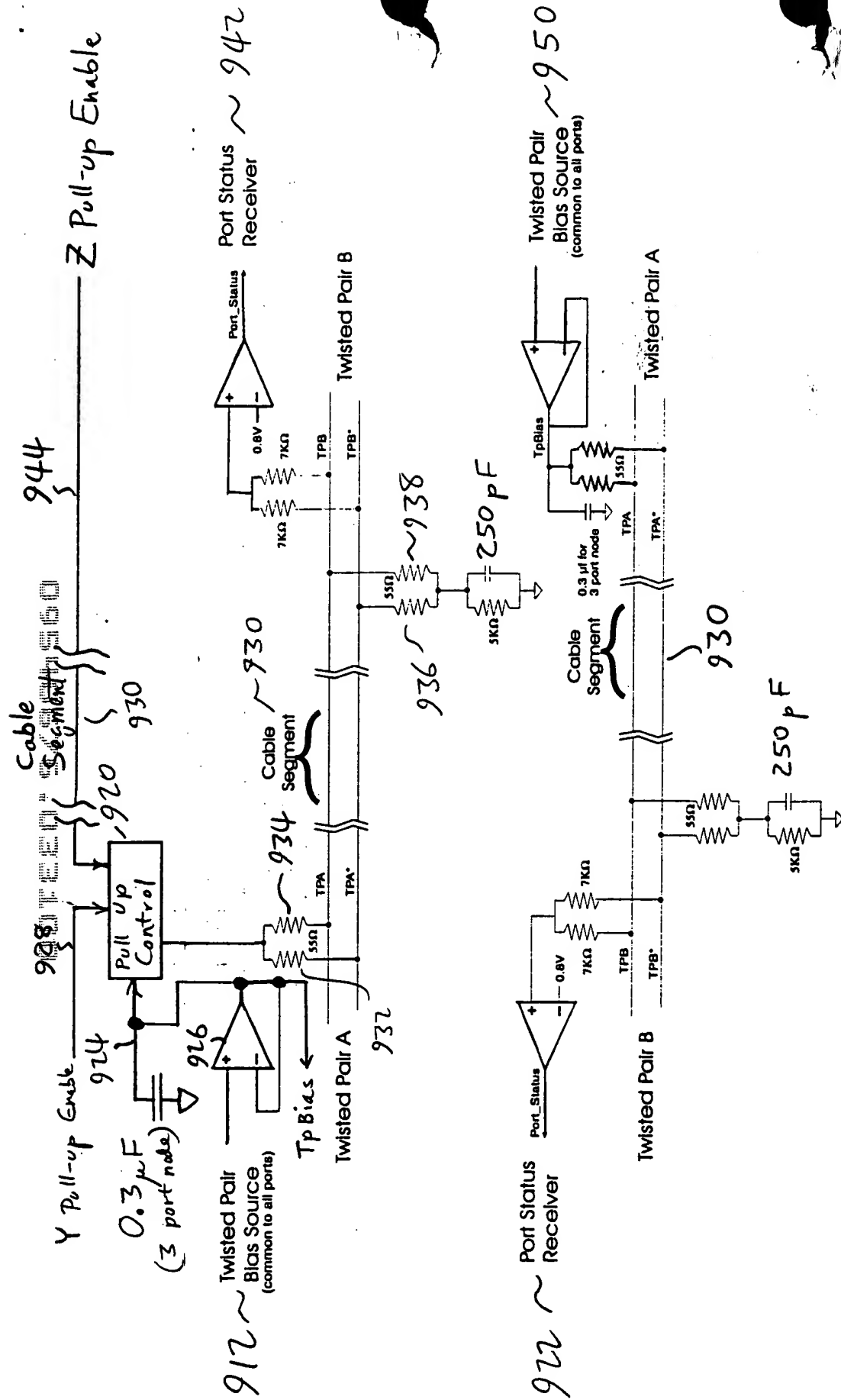


FIGURE 7



NODE Y NODE Z  
710 740  
FIGURE 8



NODE Y  
910

NODE Z  
940

FIGURE 9